Examiner Notes

STN
HCAPLUS, INSPEC, JAPIO, USPATALL
10/9/03

=> d l16 1-36 abs,bib

L16 ANSWER 1 OF 36 USPATFULL on STN
AB In a method of growing a ZnO-containing compound semiconductor single crystal, on a compound single crystal layer of a **hexagonal** crystal structure having a plurality of (0001) surfaces aligned in a sequence of terraces along a direction of a-axis, a ZnO-containing compound single crystal of a **hexagonal** crystal structure is grown, having an inclination from the c-axis toward the direction of the a-axis.

AN 2003:265073 USPATFULL
TI CRYSTAL-GROWTH SUBSTRATE AND A ZNO-CONTAINING COMPOUND SEMICONDUCTOR DEVICE
IN Kato, Hiroyuki, Tokyo, JAPAN
Sano, Michihiro, Tokyo, JAPAN
PA STANLEY ELECTRIC CO., LTD., Tokyo, JAPAN (non-U.S. corporation)
PI US 2003186088 A1 20031002
AI US 2002-260779 A1 20020927 (10)
PRAI JP 2002-86247 20020326
DT Utility
FS APPLICATION
LREP FRISHAUF, HOLTZ, GOODMAN & CHICK, PC, 767 THIRD AVENUE, 25TH FLOOR, NEW YORK, NY, 10017-2023
CLMN Number of Claims: 9
ECL Exemplary Claim: 1
DRWN 14 Drawing Page(s)
LN.CNT 894

L16 ANSWER 2 OF 36 USPATFULL on STN
AB A low dislocation density GaN single crystal substrate is made by forming a seed mask having parallel stripes regularly and periodically aligning on an undersubstrate, growing a GaN crystal on a facet-growth condition, forming repetitions of parallel facet hills and facet valleys rooted upon the mask stripes, maintaining the facet hills and facet valleys, producing voluminous defect accumulating regions (H) accompanying the valleys, yielding low dislocation single crystal regions (Z) following the facets, making C-plane growth regions (Y) following flat tops between the facets, gathering dislocations on the facets into the valleys by the action of the growing facets, reducing dislocations in the low dislocation single crystal regions (Z) and the C-plane growth regions (Y), and accumulating the dislocations in cores (S) or interfaces (K) of the voluminous defect accumulating regions (H).

CAS INDEXING IS AVAILABLE FOR THIS PATENT.
AN 2003:211160 USPATFULL
TI Single crystal GaN substrate, method of growing single crystal GaN and method of producing single crystal GaN substrate
IN Motoki, Kensaku, Hyogo, JAPAN
Hirota, Ryu, Hyogo, JAPAN
Okahisa, Takuji, Hyogo, JAPAN
Nakahata, Seiji, Hyogo, JAPAN
PA Sumitomo Electric Industries, Ltd. (non-U.S. corporation)
PI US 2003145783 A1 20030807
AI US 2002-265719 A1 20021008 (10)
PRAI JP 2001-311018 20011009
JP 2002-269387 20020917
DT Utility
FS APPLICATION
LREP McDERMOTT, WILL & EMERY, 600 13th Street, N.W., Washington, DC, 20005-3096
CLMN Number of Claims: 92

ECL Exemplary Claim: 1
DRWN 12 Drawing Page(s)
LN.CNT 3677
CAS INDEXING IS AVAILABLE FOR THIS PATENT.

L16 ANSWER 3 OF 36 USPATFULL on STN
AB The present invention provides a high efficient **nitride semiconductor** element having an opposed terminal structure, whose terminals facing each other, and a method for producing thereof.

The **nitride semiconductor** element includes a conductive layer, a first terminal, a **nitride semiconductor** with a light-emitting layer, and a second terminal, on a supporting substrate successively. The first terminal and a first insulating protect layer are interposed between the conductive layer and a first conductive type **nitride semiconductor** layer.

The method includes: a growing step for growing the **nitride semiconductor** further having an undoped GaN layer on a different material substrate; subsequently, a attaching step for attaching the supporting substrate to the first conductive type **nitride semiconductor** layer side of the **nitride semiconductor** with interposing the first terminal between them; and subsequently, an exposing step for exposing the second conductive type **nitride semiconductor** layer by eliminating the different material substrate and the undoped GaN.

CAS INDEXING IS AVAILABLE FOR THIS PATENT.
AN 2003:205159 USPATFULL
TI **Nitride semiconductor** element with a supporting substrate and a method for producing a **nitride semiconductor** element
IN Sano, Masahiko, Anan-shi, JAPAN
Nonaka, Mitsuhiro, Anan-shi, JAPAN
Kamada, Kazumi, Anan-shi, JAPAN
Yamamoto, Masashi, Anan-shi, JAPAN
PI US 2003141506 A1 20030731
AI US 2003-351497 A1 20030127 (10)
PRAI JP 2002-19192 20020128
JP 2002-195179 20020703
JP 2002-356463 20021209
JP 2002-175686 20020617
JP 2002-233866 20020809
DT Utility
FS APPLICATION
LREP WENDEROTH, LIND & PONACK, L.L.P., 2033 K STREET N. W., SUITE 800, WASHINGTON, DC, 20006-1021
CLMN Number of Claims: 29
ECL Exemplary Claim: 1
DRWN 27 Drawing Page(s)
LN.CNT 3229
CAS INDEXING IS AVAILABLE FOR THIS PATENT.

L16 ANSWER 4 OF 36 USPATFULL on STN
AB A **nitride semiconductor** light emitting device includes an emission layer (106) having a multiple quantum well structure where a plurality of quantum well layers and a plurality of barrier layers are alternately stacked. The quantum well layer is formed of XN.sub.1-x-yAs.sub.xP.sub.ySb.sub.z (0.ltoreq.x.ltoreq.0.15, 0.ltoreq.y.ltoreq.0.2, 0.ltoreq.z.ltoreq.0.05, x+y+z>0) where X represents one or more kinds of group III elements. The barrier layer is formed of a **nitride semiconductor** layer containing

at least Al.

AN 2003:198977 USPATFULL
TI **Nitride semiconductor** light-emitting device and optical apparatus including the same
IN Tsuda, Yuhzoh, Nara, JAPAN
Yuasa, Takayuki, Nara, JAPAN
Ito, Shigetoshi, Nara, JAPAN
PI US 2003136957 A1 20030724
AI US 2002-276512 A1 20021114 (10)
WO 2001-JP3825 20010507
PRAI JP 2000-158189 20000529
DT Utility
FS APPLICATION
LREP MORRISON & FOERSTER LLP, 755 PAGE MILL RD, PALO ALTO, CA, 94304-1018
CLMN Number of Claims: 18
ECL Exemplary Claim: 1
DRWN 11 Drawing Page(s)
LN.CNT 1154

L16 ANSWER 5 OF 36 USPATFULL on STN
AB A semiconductor laser device comprises a laminate consisting of a semiconductor layer of first conductivity type, an active layer and a semiconductor layer of second conductivity type, which is different from the first conductivity type, that are stacked in order, with a waveguide region being formed to guide a light beam in a direction perpendicular to the direction of width by restricting the light from spreading in the direction of width in the active layer and in the proximity thereof, wherein the waveguide region has a first waveguide region and a second waveguide region, the first waveguide region is a region where light is confined within the limited active layer by means of a difference in the refractive index between the active layer and the regions on both sides of the active layer by limiting the width of the active layer, and the second waveguide region is a region where the light is confined therein by providing effective difference in refractive index in the active layer.

CAS INDEXING IS AVAILABLE FOR THIS PATENT.
AN 2003:186944 USPATFULL
TI Semiconductor laser device, and method of manufacturing the same
IN Matsumura, Hiroaki, Tokushima, JAPAN
PI US 2003128729 A1 20030710
AI US 2002-297332 A1 20021205 (10)
WO 2001-JP3548 20010425
PRAI JP 2000-172797 20000608
JP 2001-116197 20010413
DT Utility
FS APPLICATION
LREP MORRISON & FOERSTER LLP, 1650 TYSONS BOULEVARD, SUITE 300, MCLEAN, VA, 22102
CLMN Number of Claims: 26
ECL Exemplary Claim: 1
DRWN 17 Drawing Page(s)
LN.CNT 3011
CAS INDEXING IS AVAILABLE FOR THIS PATENT.

L16 ANSWER 6 OF 36 USPATFULL on STN
AB A UV light sensing element has at least a first electrode and a sensor. The first electrode has a semiconductor containing at least one element selected from Al, Ga and In together with nitrogen or oxygen, and the sensor layer has a semiconductor containing at least one element selected from Al, Ga and In together with nitrogen. A longer wavelength end of an absorption spectrum for the first electrode is located at a

position nearer to a shorter wavelength side than a longer wavelength end of an absorption spectrum for the sensor.

CAS INDEXING IS AVAILABLE FOR THIS PATENT.
AN 2003:138837 USPATFULL
TI UV light sensing element
IN Yagi, Shigeru, Minamiashigara-shi, JAPAN
PA FUJI XEROX CO., LTD., Tokyo, JAPAN (non-U.S. corporation)
PI US 2003094664 A1 20030522
AI US 2002-93422 A1 20020311 (10)
PRAI JP 2001-357058 20011122
DT Utility
FS APPLICATION
LREP OLIFF & BERRIDGE, PLC, P.O. BOX 19928, ALEXANDRIA, VA, 22320
CLMN Number of Claims: 10
ECL Exemplary Claim: 1
DRWN 1 Drawing Page(s)
LN.CNT 1213
CAS INDEXING IS AVAILABLE FOR THIS PATENT.

L16 ANSWER 7 OF 36 USPATFULL on STN
AB To provide a method of manufacturing compound **semiconductor** single **crystals** such as silicon carbide and gallium **nitride** by epitaxial growth methods, that is capable of yielding compound single crystals of comparatively low planar defect density. The method of manufacturing compound single crystals in which two or more compound single crystalline layers identical to or differing from a single crystalline substrate are sequentially epitaxially grown on the surface of said substrate. At least a portion of said substrate surface has plural undulations extending in a single direction and second and subsequent epitaxial growth is conducted after the formation of plural undulations extending in a single direction in at least a portion of the surface of the compound single crystalline layer formed proximately.

CAS INDEXING IS AVAILABLE FOR THIS PATENT.
AN 2003:68856 USPATFULL
TI Method of manufacturing compound single crystal
IN Kawahara, Takamitsu, Kawasaki-shi, JAPAN
Nagasawa, Hiroyuki, Tokyo, JAPAN
Yagi, Kuniaki, Tokyo, JAPAN
PA HOYA CORPORATION, Tokyo, JAPAN, 161-8525 (non-U.S. corporation)
PI US 2003047129 A1 20030313
AI US 2002-227227 A1 20020826 (10)
PRAI JP 2001-256282 20010827
DT Utility
FS APPLICATION
LREP OBLON SPIVAK MCCLELLAND MAIER & NEUSTADT PC, FOURTH FLOOR, 1755 JEFFERSON DAVIS HIGHWAY, ARLINGTON, VA, 22202
CLMN Number of Claims: 7
ECL Exemplary Claim: 1
DRWN 5 Drawing Page(s)
LN.CNT 916
CAS INDEXING IS AVAILABLE FOR THIS PATENT.

L16 ANSWER 8 OF 36 USPATFULL on STN
AB A method of growing a **nitride semiconductor** **crystal** which has very few **crystal** defects and can be used as a substrate is disclosed. This invention includes the step of forming a first selective growth mask on a support member including a dissimilar substrate having a major surface and made of a material different from a **nitride semiconductor**, the first selective growth mask having a plurality of first windows for selectively exposing the upper surface of the support member, and the

step of growing **nitride semiconductor** portions from the upper surface, of the support member, which is exposed from the windows, by using a gaseous Group 3 element source and a gaseous nitrogen source, until the **nitride semiconductor** portions grown in the adjacent windows combine with each other on the upper surface of the selective growth mask.

CAS INDEXING IS AVAILABLE FOR THIS PATENT.
AN 2003:55161 USPATFULL
TI **Nitride semiconductor** growth method, **nitride semiconductor** substrate, and **nitride semiconductor** device
IN Kiyoku, Hiroyuki, Anan-shi, JAPAN
Nakamura, Shuji, Anan-shi, JAPAN
Kozaki, Tokuya, Anan-shi, JAPAN
Iwasa, Naruhito, Anan-shi, JAPAN
Chocho, Kazuyuki, Anan-shi, JAPAN
PA NICHIA CHEMICAL INDUSTRIES, LTD. (non-U.S. corporation)
PI US 2003037722 A1 20030227
AI US 2002-261487 A1 20021002 (10)
RLI Division of Ser. No. US 2001-986332, filed on 8 Nov 2001, PENDING
Continuation of Ser. No. US 2000-603437, filed on 23 Jun 2000, PENDING
Division of Ser. No. US 1998-202141, filed on 9 Dec 1998, GRANTED, Pat. No. US 6153010 A 371 of International Ser. No. WO 1998-JP1640, filed on 9 Apr 1998, UNKNOWN
PRAI JP 1997-93315 19970411
JP 1997-174494 19970630
JP 1997-181071 19970707
JP 1997-201477 19970728
JP 1997-277448 19971009
JP 1997-290098 19971022
JP 1997-324997 19971126
DT Utility
FS APPLICATION
LREP SUGHRUE MION, PLLC, 2100 Pennsylvania Avenue, NW, Washington, DC, 20037-3213
CLMN Number of Claims: 11
ECL Exemplary Claim: 1
DRWN 8 Drawing Page(s)
LN.CNT 3096
CAS INDEXING IS AVAILABLE FOR THIS PATENT.

L16 ANSWER 9 OF 36 USPATFULL on STN
AB **Nitride semiconductor** devices and methods of producing same are provided. The present invention includes forming a **nitride semiconductor** layer on a base body of the **nitride semiconductor** under selective and controlled **crystal** growth conditions. For example, the crystal growth rate, the supply of crystal growth source material and/or the crystal growth area can be varied over time, thus resulting in a **nitride semiconductor** device with enhanced properties.

CAS INDEXING IS AVAILABLE FOR THIS PATENT.
AN 2002:327998 USPATFULL
TI Vapor-phase growth method for a **nitride semiconductor** and a **nitride semiconductor** device
IN Biwa, Goshi, Kanagawa, JAPAN
Okuyama, Hiroyuki, Kanagawa, JAPAN
Doi, Masato, Kanagawa, JAPAN
Oohata, Toyoharu, Kanagawa, JAPAN
PI US 2002185660 A1 20021212
AI US 2002-126240 A1 20020418 (10)
PRAI JP 2001-120615 20010419

DT Utility
FS APPLICATION
LREP BELL, BOYD & LLOYD, LLC, P. O. BOX 1135, CHICAGO, IL, 60690-1135
CLMN Number of Claims: 27
ECL Exemplary Claim: 1
DRWN 6 Drawing Page(s)
LN.CNT 1187
CAS INDEXING IS AVAILABLE FOR THIS PATENT.

L16 ANSWER 10 OF 36 USPATFULL on STN
AB A display unit and semiconductor light emitting devices are provided. The display unit includes a number of the semiconductor light emitting devices arrayed on a base body, wherein each of the semiconductor light emitting devices is formed together with dummy devices for setting an emission wavelength of the semiconductor light emitting device, and the semiconductor light emitting device is formed by selective growth, and one conductive layer is formed in self-alignment on planes grown from tilt planes formed by selective growth. Such a display unit has a structure suitable for multi-colors without increasing the number of production steps.

AN 2002:305992 USPATFULL
TI Display unit and semiconductor light emitting device
IN Okuyama, Hiroyuki, Kanagawa, JAPAN
Doi, Masato, Kanagawa, JAPAN
Biwa, Goshi, Kanagawa, JAPAN
Oohata, Toyoharu, Kanagawa, JAPAN
Minami, Masaru, Kanagawa, JAPAN
PI US 2002171089 A1 20021121
AI US 2002-92687 A1 20020306 (10)
PRAI JP 2001-62206 20010306
JP 2001-362444 20011128
DT Utility
FS APPLICATION
LREP Bell, Boyd & Lloyd LLC, P.O. Box 1135, Chicago, IL, 60690
CLMN Number of Claims: 26
ECL Exemplary Claim: 1
DRWN 28 Drawing Page(s)
LN.CNT 2612

L16 ANSWER 11 OF 36 USPATFULL on STN
AB A low defect density (Ga,Al,In)N material. The (Ga, Al, In)N material may be of large area, crack-free character, having a defect density as low as 3.times.10.sup.6 defects/cm.sup.2 or lower. Such (Ga,Al,In)N material is useful as a substrate for epitaxial growth of Group III-V nitride device structures thereon.

CAS INDEXING IS AVAILABLE FOR THIS PATENT.
AN 2002:298981 USPATFULL
TI Low defect density (Ga, Al, In) N and HVPE process for making same
IN Vaudo, Robert P., New Milford, CT, UNITED STATES
Phanse, Vivek M., Cambridge, MA, UNITED STATES
Tischler, Michael A., Phoenix, AZ, UNITED STATES
PI US 2002166502 A1 20021114
AI US 2002-103226 A1 20020321 (10)
RLI Continuation of Ser. No. US 1998-179049, filed on 26 Oct 1998, PENDING Continuation-in-part of Ser. No. US 1997-984473, filed on 3 Dec 1997, GRANTED, Pat. No. US 6156581 Continuation-in-part of Ser. No. US 1997-955168, filed on 21 Oct 1997, ABANDONED Continuation-in-part of Ser. No. US 1994-188469, filed on 27 Jan 1994, GRANTED, Pat. No. US 5679152
PRAI US 1997-63249P 19971024 (60)
US 1996-31555P 19961203 (60)

DT Utility
FS APPLICATION
LREP ATMI, INC., 7 COMMERCE DRIVE, DANBURY, CT, 06810
CLMN Number of Claims: 109
ECL Exemplary Claim: 63
DRWN 13 Drawing Page(s)
LN.CNT 1616
CAS INDEXING IS AVAILABLE FOR THIS PATENT.

L16 ANSWER 12 OF 36 USPATFULL on STN
AB A silicon nitride sintered body comprising Mg and at least one rare earth element selected from the group consisting of La, Y, Gd and Yb, the total oxide-converted content of the above elements being 0.6-7 weight %, with Mg converted to MgO and rare earth elements converted to rare earth oxides RE.sub.xO.sub.y. The silicon nitride sintered body is produced by mixing 1-50 parts by weight of a first silicon nitride powder having a .beta.-particle ratio of 30-100%, an oxygen content of 0.5 weight % or less, an average particle size of 0.2-10 .mu.m, and an aspect ratio of 10 or less, with 99-50 parts by weight of .alpha.-silicon nitride powder having an average particle size of 0.2-4 .mu.m; and sintering the resultant mixture at a temperature of 1,800.degree. C. or higher and pressure of 5 atm or more in a nitrogen atmosphere.

CAS INDEXING IS AVAILABLE FOR THIS PATENT.
AN 2002:294433 USPATFULL
TI Silicon nitride powder, silicon nitride sintered body, sintered silicon nitride substrate, and circuit board and thermoelectric module comprising such sintered silicon nitride substrate
IN Imamura, Hisayuki, Saitama-ken, JAPAN
Hamayoshi, Shigeyuki, Fukuoka-ken, JAPAN
Kawata, Tsunehiro, Saitama-ken, JAPAN
Sobue, Masahisa, Saitama-ken, JAPAN
PA HITACHI METALS, LTD. (non-U.S. corporation)
PI US 2002164475 A1 20021107
AI US 2001-956033 A1 20010920 (9)
PRAI JP 2000-284957 20000920
JP 2000-326489 20001026
DT Utility
FS APPLICATION
LREP SUGHRUE MION ZINN MACPEAK & SEAS, PLLC, 2100 Pennsylvania Avenue, NW, Washington, DC, 20037-3213
CLMN Number of Claims: 19
ECL Exemplary Claim: 1
DRWN 8 Drawing Page(s)
LN.CNT 1772
CAS INDEXING IS AVAILABLE FOR THIS PATENT.

L16 ANSWER 13 OF 36 USPATFULL on STN
AB A GaN single crystal is grown by synthesizing GaN in vapor phase, piling a GaN crystal on a substrate, producing a three-dimensional facet structure including facets in the GaN crystal without making a flat surface, maintaining the facet structure without burying the facet structure, and reducing dislocations in the growing GaN crystal. The facet structure reduces the EPD down to less than 10.sup.6 cm.sup.-2.

CAS INDEXING IS AVAILABLE FOR THIS PATENT.
AN 2002:275595 USPATFULL
TI Method of growing single crystal GaN, method of making single crystal GaN substrate and single crystal GaN substrate
IN Motoki, Kensaku, Itami, JAPAN
Okahisa, Takuji, Itami, JAPAN
Matsumoto, Naoki, Itami, JAPAN

PA Sumitomo Electric Industries Ltd., Osaka, JAPAN (non-U.S. corporation)
PI US 6468347 B1 20021022
AI US 2000-669840 20000927 (9)
PRAI JP 1999-273882 19990928
DT Utility
FS GRANTED
EXNAM Primary Examiner: Kunemund, Robert
LREP Smith, Gambrell & Russell, LLP
CLMN Number of Claims: 51
ECL Exemplary Claim: 1
DRWN 31 Drawing Figure(s); 10 Drawing Page(s)
LN.CNT 2566
CAS INDEXING IS AVAILABLE FOR THIS PATENT.

L16 ANSWER 14 OF 36 USPATFULL on STN
AB A method for manufacturing a **nitride semiconductor** device in which **nitride crystals** are sequentially grown on a substrate such as sapphire by MOCVD or the like, and p electrode and n electrode are formed. The wafer is not cut along two perpendicular directions, but rather is cut along two directions that form a 120 **degree angle**, to obtain a rhombus shaped semiconductor chip. Because the wafer has a six-fold rotation symmetry, by cutting the wafer at an angle of 120 degrees, the cutting directions are equivalent and the wafer can be cut in directions along which it can be easily split.

CAS INDEXING IS AVAILABLE FOR THIS PATENT.
AN 2002:232645 USPATFULL
TI **Nitride semiconductor** chip and method for manufacturing **nitride semiconductor** chip
IN Sakai, Shiro, Tokushima-shi, JAPAN
Lacroix, Yves, Tokushima-shi, JAPAN
PI US 2002124794 A1 20020912
AI US 2002-44686 A1 20020111 (10)
PRAI JP 2001-3910 20010111
DT Utility
FS APPLICATION
LREP ROSENTHAL & OSHA L.L.P., 1221 MCKINNEY AVENUE, SUITE 2800, HOUSTON, TX, 77010
CLMN Number of Claims: 11
ECL Exemplary Claim: 1
DRWN 4 Drawing Page(s)
LN.CNT 293
CAS INDEXING IS AVAILABLE FOR THIS PATENT.

L16 ANSWER 15 OF 36 USPATFULL on STN
AB LEDs employing a III-Nitride light emitting active region deposited on a base layer above a substrate show improved optical properties with the base layer grown on an intentionally misaligned substrate with a thickness greater than 3.5 .mu.m. Improved brightness, improved quantum efficiency, and a reduction in the current at which maximum quantum efficiency occurs are among the improved optical properties resulting from use of a misaligned substrate and a thick base layer. Illustrative examples are given of misalignment **angles** in the range from 0.05.**degree**. to 0.50.degree., and base layers in the range from 6.5 to 9.5 .mu.m although larger values of both misalignment angle and base layer thickness can be used. In some cases, the use of thicker base layers provides sufficient structural support to allow the substrate to be removed from the device entirely.

CAS INDEXING IS AVAILABLE FOR THIS PATENT.
AN 2002:226513 USPATFULL
TI Increasing the brightness of III-nitride light emitting devices

IN Khare, Reena, Sunnyvale, CA, UNITED STATES
Goetz, Werner K., Palo Alto, CA, UNITED STATES
Camras, Michael D., Sunnyvale, CA, UNITED STATES
PI US 2002121646 A1 20020905
US 6576932 B2 20030610
AI US 2001-797770 A1 20010301 (9)
DT Utility
FS APPLICATION
LREP Brian D. Ogonowsky, SKJERVEN MORRILL MacPHERSON LLP, Suite 700, 25 Metro Drive, San Jose, CA, 95110-1349
CLMN Number of Claims: 26
ECL Exemplary Claim: 1
DRWN 9 Drawing Page(s)
LN.CNT 560
CAS INDEXING IS AVAILABLE FOR THIS PATENT.

L16 ANSWER 16 OF 36 USPATFULL on STN
AB Semiconductor light-emitting devices are provided. The semiconductor light-emitting devices include a substrate and a crystal layer selectively grown thereon at least a portion of the crystal layer is oriented along a plane that slants to or diagonally intersect a principal plane of orientation associated with the substrate thereby for example, enhancing crystal properties, preventing threading dislocations, and facilitating device miniaturization and separation during manufacturing and use thereof

CAS INDEXING IS AVAILABLE FOR THIS PATENT.
AN 2002:219556 USPATFULL
TI Semiconductor light-emitting device and process for producing the same
IN Okuyama, Hiroyuki, Kanagawa, JAPAN
Doi, Masato, Kanagawa, JAPAN
Biwa, Goshi, Kanagawa, JAPAN
Oohata, Toyoharu, Kanagawa, JAPAN
Kikutani, Tomoyuki, Kanagawa, JAPAN
PI US 2002117677 A1 20020829
AI US 2002-62687 A1 20020130 (10)
RLI Continuation of Ser. No. WO 2001-JP6212, filed on 18 Jul 2001, UNKNOWN
PRAI JP 2000-218034 20000718
JP 2000-217663 20000718
JP 2000-217508 20000718
JP 2000-217799 20000718
JP 2000-218101 20000718
JP 2001-200183 20010629
DT Utility
FS APPLICATION
LREP BELL, BOYD & LLOYD, LLC, P. O. BOX 1135, CHICAGO, IL, 60690-1135
CLMN Number of Claims: 82
ECL Exemplary Claim: 1
DRWN 71 Drawing Page(s)
LN.CNT 4170
CAS INDEXING IS AVAILABLE FOR THIS PATENT.

L16 ANSWER 17 OF 36 USPATFULL on STN
AB A semiconductor laser device includes an n-GaN substrate as a first **semiconductor** layer, a layered lump of **hexagonal nitride**-based **semiconductor** layers provided as a second **semiconductor** layer on an upper side of the first semiconductor layer, a mirror end face formed by cleavage such that both of the n-GaN substrate and layered lump have their side surfaces exposed on the approximately same plane, and a buffer layer provided between the n-GaN substrate and the layered lump. On the mirror end face, the value of an average roughness of an exposed portion of the layered lump is a half or lower compared to an average roughness of an exposed portion of

the n-GaN substrate.

CAS INDEXING IS AVAILABLE FOR THIS PATENT.
AN 2002:197897 USPATFULL
TI Semiconductor laser device and method of manufacturing the same
IN Yamasaki, Yukio, Osaka, JAPAN
PI US 2002105986 A1 20020808
AI US 2001-28175 A1 20011220 (10)
PRAI JP 2000-386992 20001220
DT Utility
FS APPLICATION
LREP MORRISON & FOERSTER LLP, 755 PAGE MILL RD, PALO ALTO, CA, 94304-1018
CLMN Number of Claims: 10
ECL Exemplary Claim: 1
DRWN 21 Drawing Page(s)
LN.CNT 1433
CAS INDEXING IS AVAILABLE FOR THIS PATENT.

L16 ANSWER 18 OF 36 USPATFULL on STN
AB A **nitride semiconductor** light emitting device includes a worked substrate including grooves and lands formed on a main surface of a **nitride semiconductor** substrate, a **nitride semiconductor** underlayer covering the grooves and the lands of the worked substrate and a **nitride semiconductor** multilayer emission structure including an emission layer including a quantum well layer or both a quantum well layer and a barrier layer in contact with the quantum well layer between an n-type layer and a p-type layer over the **nitride semiconductor** underlayer, while the width of the grooves is within the range of 11 to 30 .mu.m and the width of the lands is within the range of 1 to 20 .mu.m.

CAS INDEXING IS AVAILABLE FOR THIS PATENT.
AN 2002:111119 USPATFULL
TI **Nitride semiconductor** light emitting device and apparatus including the same
IN Tsuda, Yuhzoh, Nara, JAPAN
Yuasa, Takayuki, Nara, JAPAN
Ito, Shigetoshi, Nara, JAPAN
Taneya, Mototaka, Nara, JAPAN
PI US 2002056846 A1 20020516
US 6452216 B2 20020917
AI US 2001-952845 A1 20010911 (9)
PRAI JP 2000-344847 20001113
DT Utility
FS APPLICATION
LREP Thomas E. Ciotti, Morrison & Foester LLP, 755 Page Mill Rd., Palo Alto, CA, 94301-1018
CLMN Number of Claims: 11
ECL Exemplary Claim: 1
DRWN 10 Drawing Page(s)
LN.CNT 1178
CAS INDEXING IS AVAILABLE FOR THIS PATENT.

L16 ANSWER 19 OF 36 USPATFULL on STN
AB A **nitride semiconductor** laser device having a low threshold current and low noise is provided. The laser device includes n-type and p-type layers made of **nitride semiconductor** and formed on a substrate, and a light emitting layer between the n-type and p-type layers. The light emitting layer is formed of a well layer or a combination of well and barrier layers. At least the well layer is made of **nitride semiconductor** containing element X, N and Ga, wherein element is at least one selected from the group

consisting of As, P and Sb. The atomic fraction of element X is smaller than that of N. A maximum width through which current is injected into the light emitting layer via the p-type layer is from 1.0 .mu.m to 4.0 .mu.m.

CAS INDEXING IS AVAILABLE FOR THIS PATENT.
AN 2002:105416 USPATFULL
TI **Nitride semiconductor** laser device and optical device using the same
IN Tsuda, Yuhzoh, Tenri-shi, JAPAN
Ito, Shigetoshi, Ikoma-shi, JAPAN
Okumura, Toshiyuki, Tenri-shi, JAPAN
PI US 2002054617 A1 20020509
US 6614824 B2 20030902
AI US 2001-950576 A1 20010913 (9)
PRAI JP 2000-279207 20000914
DT Utility
FS APPLICATION
LREP BIRCH STEWART KOLASCH & BIRCH, PO BOX 747, FALLS CHURCH, VA, 22040-0747
CLMN Number of Claims: 10
ECL Exemplary Claim: 1
DRWN 12 Drawing Page(s)
LN.CNT 1319
CAS INDEXING IS AVAILABLE FOR THIS PATENT.

L16 ANSWER 20 OF 36 USPATFULL on STN
AB A buffer layer 602 and a gallium nitride contact layer 603 are formed on a sapphire (0001) plane substrate 101 by a MOVPE process, and then a silicon nitride mask 102 is formed on the surface. On the silicon nitride mask 102 is formed a rectangular opening whose longer and shorter sides are in the directions of [11-20] and [1-100] of the gallium **nitride**. On the opening is formed a gallium **nitride semiconductor** layer 104 by a MOVPE process, whose side face, the (11-20) plane is used as a resonator end face 103.

CAS INDEXING IS AVAILABLE FOR THIS PATENT.
AN 2002:91785 USPATFULL
TI GALLIUM **NITRIDE SEMICONDUCTOR** LASER AND A MANUFACTURING PROCESS THEREOF
IN KIMURA, AKITAKA, TOKYO, JAPAN
PI US 2002048302 A1 20020425
AI US 1998-98433 A1 19980617 (9)
PRAI JP 1997-162717 19970619
DT Utility
FS APPLICATION
LREP SUGHRUE MION ZINN MACPEAK & SEAS, 2100 PENNSYLVANIA AVENUE NW, WASHINGTON, DC, 200373202
CLMN Number of Claims: 9
ECL Exemplary Claim: 1
DRWN 3 Drawing Page(s)
LN.CNT 546
CAS INDEXING IS AVAILABLE FOR THIS PATENT.

L16 ANSWER 21 OF 36 USPATFULL on STN
AB An object of the present invention is to improve, in a group III **nitride semiconductor** device, the productivity, heat radiation characteristic and performance in the element high speed operation; upon a sapphire substrate in which an A plane (an (11-20) plane) is set to be the basal plane, an epitaxial growth layer of a group III **nitride semiconductor** is formed and, thereon, a gate electrode 16, a source electrode 15 and a drain electrode 17 are formed; these electrodes are disposed in such a way that a direction along which they are laid makes an **angle**

within 20.**degree**. with respect to a C axis of sapphire.

CAS INDEXING IS AVAILABLE FOR THIS PATENT.
AN 2002:90623 USPATFULL
TI Semiconductor device
IN Ohno, Yasuo, Tokyo, JAPAN
Hayama, Nobuyuki, Tokyo, JAPAN
Kasahara, Kensuke, Tokyo, JAPAN
Nakayama, Tatsuo, Tokyo, JAPAN
Miyamoto, Hironobu, Tokyo, JAPAN
Takahashi, Yuji, Tokyo, JAPAN
Ando, Yuji, Tokyo, JAPAN
Matsunaga, kohji, Tokyo, JAPAN
Kuzuhara, Masaaki, Tokyo, JAPAN
PA NEC CORPORATION (non-U.S. corporation)
PI US 2002047113 A1 20020425
US 6441391 B2 20020827
AI US 2001-940374 A1 20010829 (9)
PRAI JP 2000-265783 20000901
DT Utility
FS APPLICATION
LREP SUGHRUE MION ZINN MACPEAK & SEAS, PLLC, 2100 Pennsylvania Avenue, NW, Washington, DC, 20037-3202
CLMN Number of Claims: 3
ECL Exemplary Claim: 1
DRWN 5 Drawing Page(s)
LN.CNT 659
CAS INDEXING IS AVAILABLE FOR THIS PATENT.

L16 ANSWER 22 OF 36 USPATFULL on STN
AB A method of growing a **nitride semiconductor** **crystal** which has very few **crystal** defects and can be used as a substrate is disclosed. This invention includes the step of forming a first selective growth mask on a support member including a dissimilar substrate having a major surface and made of a material different from a **nitride semiconductor**, the first selective growth mask having a plurality of first windows for selectively exposing the upper surface of the support member, and the step of growing **nitride semiconductor** portions from the upper surface, of the support member, which is exposed from the windows, by using a gaseous Group 3 element source and a gaseous nitrogen source, until the **nitride semiconductor** portions grown in the adjacent windows combine with each other on the upper surface of the selective growth mask.

CAS INDEXING IS AVAILABLE FOR THIS PATENT.
AN 2002:90208 USPATFULL
TI **Nitride semiconductor** growth method, **nitride** **semiconductor** substrate, and **nitride** **semiconductor** device
IN Kiyoku, Hiroyuki, Anan-shi, JAPAN
Nakamura, Shuji, Anan-shi, JAPAN
Kozaki, Tokuya, Anan-shi, JAPAN
Iwasa, Naruhito, Anan-shi, JAPAN
Chocho, Kazuyuki, Anan-shi, JAPAN
PA NICHIA CHEMICAL INDUSTRIES, LTD. (non-U.S. corporation)
PI US 2002046693 A1 20020425
AI US 2001-986332 A1 20011108 (9)
RLI Continuation of Ser. No. US 2000-603437, filed on 23 Jun 2000, PENDING
Division of Ser. No. US 1998-202141, filed on 9 Dec 1998, PATENTED A 371 of International Ser. No. WO 1998-JP1640, filed on 9 Apr 1998, UNKNOWN
PRAI JP 1997-93315 19970411
JP 1997-174494 19970630

JP 1997-181071 19970707
JP 1997-201477 19970728
JP 1997-277448 19971009
JP 1997-290098 19971022
JP 1997-324997 19971126
DT Utility
FS APPLICATION
LREP SUGHRUE MION, PLLC, 2100 Pennsylvania Avenue, NW, Washington, DC, 20037-3213
CLMN Number of Claims: 186
ECL Exemplary Claim: 1
DRWN 8 Drawing Page(s)
LN.CNT 3709
CAS INDEXING IS AVAILABLE FOR THIS PATENT.

L16 ANSWER 23 OF 36 USPATFULL on STN
AB A GaN crystal film having a mask patterned in a stripe for forming multiple growing areas on a sapphire substrate and coalesced GaN crystals covering the mask dividing the areas, grown from the neighboring growing areas, comprising defects where multiple dislocations along with the stripe are substantially aligned with the normal line of the substrate, in the crystal areas over the mask, and dislocations propagating in substantially parallel with the substrate surface while, in the vicinity of the areas where the crystals are coalesced over the mask, propagating substantially in the normal line of the substrate surface, and a manufacturing process therefor. According to this invention, there can be provided a GaN crystal film in which strain, defects and dislocations are reduced and which tends not to generate cracks.

CAS INDEXING IS AVAILABLE FOR THIS PATENT.
AN 2001:98280 USPATFULL
TI GaN **crystal** film, a group III element **nitride** **semiconductor** wafer and a manufacturing process therefor
IN Usui, Akira, Tokyo, Japan
Sakai, Akira, Tokyo, Japan
Sunakawa, Haruo, Tokyo, Japan
Mizuta, Masashi, Tokyo, Japan
Matsumoto, Yoshishige, Tokyo, Japan
PA NEC Corporation, Tokyo, Japan (non-U.S. corporation)
PI US 6252261 B1 20010626
AI US 1999-342003 19990628 (9)
PRAI JP 1998-291354 19980930
JP 1999-122816 19990326
DT Utility
FS GRANTED
EXNAM Primary Examiner: Clark, Sheila V.
LREP Hutchins, Wheeler & Dittmar
CLMN Number of Claims: 61
ECL Exemplary Claim: 1
DRWN 29 Drawing Figure(s); 15 Drawing Page(s)
LN.CNT 2152
CAS INDEXING IS AVAILABLE FOR THIS PATENT.

L16 ANSWER 24 OF 36 USPATFULL on STN
AB A method of growing a group III **nitride semiconductor** **crystal** layer includes a step of growing a first buffer layer composed of boron phosphide on a silicon single crystal substrate by a vapor phase growth method at a temperature of not lower than 200.degree. C. and not higher than 700.degree. C., a step of growing a second buffer layer composed of boron phosphide on the first buffer layer by a vapor phase growth method at a temperature of not lower than 750.degree. C. and not higher than 1200.degree. C., and a step of growing a

crystal layer composed of group III **nitride** **semiconductor crystal** represented by general formula Al.sub.p Ga.sub.q In.sub.r N (where 0.ltoreq.p.ltoreq.1, 0.ltoreq.q.ltoreq.1, 0.ltoreq.r.ltoreq.1, p+q+r=1) on the second buffer layer by a vapor phase growth method. A **semiconductor** device incorporating the group III **nitride semiconductor** **crystal** layer is provided.

CAS INDEXING IS AVAILABLE FOR THIS PATENT.
AN 2001:29894 USPATFULL
TI Method of growing group III **nitride semiconductor** **crystal** layer and **semiconductor** device incorporating group III **nitride semiconductor crystal** layer
IN Udagawa, Takashi, Chichibu, Japan
Terashima, Kazutaka, Ebina, Japan
Nishimura, Suzuka, Yamaguchi, Japan
Tsuzaki, Takuji, Matsumoto, Japan
PA Showa Denko Kabushiki Kaisha, Tokyo, Japan (non-U.S. corporation)
PI US 6194744 B1 20010227
AI US 2000-500450 20000209 (9)
RLI Division of Ser. No. US 1999-270749, filed on 17 Mar 1999, now patented, Pat. No. US 6069021
PRAI JP 1998-66769 19980317
JP 1999-36830 19990216
DT Utility
FS Granted
EXNAM Primary Examiner: Chaudhuri, Olik; Assistant Examiner: Wille, Douglas A.
LREP Sughrue, Mion, Zinn, Macpeak & Seas, PLLC
CLMN Number of Claims: 6
ECL Exemplary Claim: 1
DRWN 3 Drawing Figure(s); 3 Drawing Page(s)
LN.CNT 959
CAS INDEXING IS AVAILABLE FOR THIS PATENT.

L16 ANSWER 25 OF 36 USPATFULL on STN
AB A method of growing atomically-flat surfaces and high quality low-defect crystal films of semiconductor materials and fabricating improved devices thereon. The method is also suitable for growing films heteroepitaxially on substrates that are different than the film. The method is particularly suited for growth of elemental semiconductors (such as Si), compounds of Groups III and V elements of the Periodic Table (such as GaN), and compounds and alloys of Group IV elements of the Periodic Table (such as SiC).

CAS INDEXING IS AVAILABLE FOR THIS PATENT.
AN 2000:174502 USPATFULL
TI Method for growth of crystal surfaces and growth of heteroepitaxial single crystal films thereon
IN Powell, J. Anthony, North Olmsted, OH, United States
Larkin, David J., Valley City, OH, United States
Neudeck, Philip G., Olmsted Falls, OH, United States
Matus, Lawrence G., Amherst, OH, United States
PA The United States of America as represented by the Administrator of the National Aeronautics and Space Administration, Washington, DC, United States (U.S. corporation)
PI US 6165874 20001226
AI US 1998-252623 19981216 (9)
RLI Continuation-in-part of Ser. No. US 1997-887804, filed on 3 Jul 1997, now patented, Pat. No. US 5915194
DT Utility
FS Granted
EXNAM Primary Examiner: Elms, Richard; Assistant Examiner: Smith, Bradley K.

CLMN Number of Claims: 17
ECL Exemplary Claim: 1
DRWN 11 Drawing Figure(s); 8 Drawing Page(s)
LN.CNT 1680
CAS INDEXING IS AVAILABLE FOR THIS PATENT.

L16 ANSWER 26 OF 36 USPATFULL on STN
AB A method of growing a **nitride semiconductor** **crystal** which has very few **crystal** defects and can be used as a substrate is disclosed. This invention includes the step of forming a first selective growth mask on a support member including a dissimilar substrate having a major surface and made of a material different from a **nitride semiconductor**, the first selective growth mask having a plurality of first windows for selectively exposing the upper surface of the support member, and the step of growing **nitride semiconductor** portions from the upper surface, of the support member, which is exposed from the windows, by using a gaseous Group 3 element source and a gaseous nitrogen source, until the **nitride semiconductor** portions grown in the adjacent windows combine with each other on the upper surface of the selective growth mask.

CAS INDEXING IS AVAILABLE FOR THIS PATENT.
AN 2000:160409 USPATFULL
TI Method of growing **nitride** semiconductors, **nitride** **semiconductor** substrate and **nitride** **semiconductor** device
IN Kiyoku, Hiroyuki, Anan, Japan
Nakamura, Shuji, Anan, Japan
Kozaki, Tokuya, Anan, Japan
Iwasa, Naruhito, Anan, Japan
Chocho, Kazuyuki, Anan, Japan
PA Nichia Chemical Industries Ltd., Tokushima-ken, Japan (non-U.S. corporation)
PI US 6153010 20001128
WO 9847170 19981022
AI US 1998-202141 19981209 (9)
WO 1998-JP1640 19980409
19981209 PCT 371 date
19981209 PCT 102(e) date
PRAI JP 1997-93315 19970411
JP 1997-174494 19970630
JP 1997-181071 19970707
JP 1997-201477 19970728
JP 1997-277448 19971009
JP 1997-290098 19971022
JP 1997-324997 19971126
DT Utility
FS Granted
EXNAM Primary Examiner: Utech, Benjamin L.; Assistant Examiner: Anderson, Matt
LREP Nixon & Vanderhye
CLMN Number of Claims: 30
ECL Exemplary Claim: 1
DRWN 21 Drawing Figure(s); 8 Drawing Page(s)
LN.CNT 3124
CAS INDEXING IS AVAILABLE FOR THIS PATENT.

L16 ANSWER 27 OF 36 USPATFULL on STN
AB An LiGaO.sub.2 single crystal manufactured by the Czochralski method has a crystallographic axis as a pulling direction set within an **angle** range of 30.**degree**. from a b- or a-axis direction. An LiGaO.sub.2 single-crystal substrate and a method of manufacturing the single crystal and the substrate are also disclosed.

CAS INDEXING IS AVAILABLE FOR THIS PATENT.
AN 2000:76860 USPATFULL
TI LiGaO.sub.2 single crystal, single-crystal substrate, and method of manufacturing the same
IN Ishii, Takao, Kanagawa, Japan
Miyazawa, Shintaro, Kanagawa, Japan
Tazou, Yasuo, Tokyo, Japan
PA Nippon Telegraph and Telephone Corporation, Japan (non-U.S. corporation)
PI US 6077342 20000620
AI US 1999-296899 19990422 (9)
RLI Division of Ser. No. US 1998-14305, filed on 27 Jan 1998, now patented, Pat. No. US 5924229
PRAI JP 1997-33262 19970130
JP 1997-69597 19970324
DT Utility
FS Granted
EXNAM Primary Examiner: Hiteshew, Felisa
LREP Townsend and Townsend and Crew LLP, Allen, Kenneth R.
CLMN Number of Claims: 8
ECL Exemplary Claim: 1
DRWN 7 Drawing Figure(s); 2 Drawing Page(s)
LN.CNT 467
CAS INDEXING IS AVAILABLE FOR THIS PATENT.

L16 ANSWER 28 OF 36 USPATFULL on STN
AB A method of growing a group III **nitride semiconductor crystal** layer includes a step of growing a first buffer layer composed of boron phosphide on a silicon single crystal substrate by a vapor phase growth method at a temperature of not lower than 200.degree. C. and not higher than 700.degree. C., a step of growing a second buffer layer composed of boron phosphide on the first buffer layer by a vapor phase growth method at a temperature of not lower than 750.degree. C. and not higher than 1200.degree. C., and a step of growing a **crystal** layer composed of group III **nitride semiconductor crystal** represented by general formula Al.sub.p Ga.sub.q In.sub.r N (where 0.ltoreq.p.ltoreq.1, 0.ltoreq.q.ltoreq.1, 0.ltoreq.r.ltoreq.1, p+q+r=1) on the second buffer layer by a vapor phase growth method. A **semiconductor** device incorporating the group III **nitride semiconductor crystal** layer is provided.

CAS INDEXING IS AVAILABLE FOR THIS PATENT.
AN 2000:67610 USPATFULL
TI Method of growing group III **nitride semiconductor crystal** layer and **semiconductor** device incorporating group III **nitride semiconductor crystal** layer
IN Terashima, Kazutaka, Ebina, Japan
Nishimura, Suzuka, Yamaguchi, Japan
Tsuzaki, Takuji, Matsumoto, Japan
Udagawa, Takashi, Chichibu, Japan
PA Showa Denko K.K., Tokyo, Japan (non-U.S. corporation)
PI US 6069021 20000530
AI US 1999-270749 19990317 (9)
PRAI JP 1998-66769 19980317
JP 1998-180921 19980626
JP 1998-193125 19980708
JP 1998-232279 19980806
JP 1999-36830 19990216
US 1999-119326P 19990209 (60)
DT Utility
FS Granted

EXNAM Primary Examiner: Chaudhuri, Olik; Assistant Examiner: Wille, Douglas A.
LREP Sughrue, Mion, Zinn, Macpeak & Seas, PLLC
CLMN Number of Claims: 10
ECL Exemplary Claim: 1
DRWN 3 Drawing Figure(s); 3 Drawing Page(s)
LN.CNT 988
CAS INDEXING IS AVAILABLE FOR THIS PATENT.

L16 ANSWER 29 OF 36 USPATFULL on STN
AB A substrate structure includes a single crystal Si substrate and a surface layer, with a buffer layer interleaved therebetween. The buffer layer includes at least one of an R--Zr family oxide thin film composed mainly of a rare earth oxide and/or zirconium oxide, an AMnO.sub.3 thin film composed mainly of rare earth element A, Mn and O and having a **hexagonal** YMnO.sub.3 type structure, an AlO.sub.x thin film composed mainly of Al and O, and a NaCl type nitride thin film composed mainly of titanium nitride, niobium nitride, tantalum nitride or zirconium nitride. The surface layer is an epitaxial film containing a wurtzite type oxide and/or nitride. The surface layer can serve as a functional film such as a semiconductor film or an underlying film therefor, and the substrate structure is useful for the manufacture of electronic devices.

CAS INDEXING IS AVAILABLE FOR THIS PATENT.
AN 2000:40471 USPATFULL
TI Substrate structures for electronic devices
IN Yano, Yoshihiko, Kanagawa, Japan
Noguchi, Takao, Chiba, Japan
PA TDK Corporation, Tokyo, Japan (non-U.S. corporation)
PI US 6045626 20000404
AI US 1998-102568 19980623 (9)
PRAI JP 1997-202409 19970711
JP 1998-16368 19980112
JP 1998-167686 19980601
DT Utility
FS Granted
EXNAM Primary Examiner: Chaudhari, Chandra; Assistant Examiner: Christianson, Keith
LREP Oblon, Spivak, McClelland, Maier & Neustadt, P.C.
CLMN Number of Claims: 6
ECL Exemplary Claim: 1
DRWN 21 Drawing Figure(s); 10 Drawing Page(s)
LN.CNT 1597
CAS INDEXING IS AVAILABLE FOR THIS PATENT.

L16 ANSWER 30 OF 36 USPATFULL on STN
AB An LiGaO.sub.2 single crystal manufactured by the Czochralski method has a crystallographic axis as a pulling direction set within an **angle** range of 30.**degree**. from a b- or a-axis direction. An LiGaO.sub.2 single-crystal substrate and a method of manufacturing the single crystal and the substrate are also disclosed.

CAS INDEXING IS AVAILABLE FOR THIS PATENT.
AN 2000:40456 USPATFULL
TI Method of manufacturing a LiGaO.sub.2 single-crystal substrate
IN Ishii, Takao, Kanagawa, Japan
Miyazawa, Shintaro, Kanagawa, Japan
Tazou, Yasuo, Tokyo, Japan
PA Nippon Telegraph and Telephone Corporation, Tokyo, Japan (non-U.S. corporation)
PI US 6045611 20000404
AI US 1998-14308 19980127 (9)
PRAI JP 1997-33262 19970130

JP 1997-69597 19970324
DT Utility
FS Granted
EXNAM Primary Examiner: Hiteshew, Felisa
LREP Townsend and Townsend and Crew LLP
CLMN Number of Claims: 16
ECL Exemplary Claim: 1
DRWN 8 Drawing Figure(s); 2 Drawing Page(s)
LN.CNT 515
CAS INDEXING IS AVAILABLE FOR THIS PATENT.

L16 ANSWER 31 OF 36 USPATFULL on STN
AB A wedge-like etching groove is formed so that stresses can be collected along a cleavage surface of a **nitride** based compound **semiconductor**, and end portions are separated from a substrate. With these operations, a light-emitting layer can form an excellent mirror by a natural cleavage. Further, by separating a portion of the end surfaces from the substrate, it is possible to suppress a deformation from the substrate and therefore, a deterioration due to the deformation can be prevented. Therefore, it is possible to provide a **nitride** based compound **semiconductor** light-emitting device which can form an excellent cleavage surface with a simple process.

CAS INDEXING IS AVAILABLE FOR THIS PATENT.
AN 1999:132618 USPATFULL
TI **Nitride** based compound **semiconductor** light emitting device and method for producing the same
IN Saito, Shinji, Yokohama, Japan
Rennie, John, Bunkyo-ku, Japan
Onomura, Masaaki, Kawasaki, Japan
Hatakoshi, Genichi, Yokohama, Japan
PA Kabushiki Kaisha Toshiba, Kawasaki, Japan (non-U.S. corporation)
PI US 5972730 19991026
AI US 1997-937160 19970925 (8)
PRAI JP 1996-254960 19960926
DT Utility
FS Granted
EXNAM Primary Examiner: Dutton, Brian
LREP Oblon, Spivak, McClelland, Maier & Neustadt, P.C.
CLMN Number of Claims: 12
ECL Exemplary Claim: 1
DRWN 22 Drawing Figure(s); 16 Drawing Page(s)
LN.CNT 985
CAS INDEXING IS AVAILABLE FOR THIS PATENT.

L16 ANSWER 32 OF 36 USPATFULL on STN
AB A method of growing atomically-flat surfaces and high-quality low-defect crystal films of polytypic compounds heteroepitaxially on polytypic compound substrates that are different than the crystal film. The method is particularly suited for the growth of 3C-SiC, 2H-AlN, and 2H-GaN on 6H-SiC.

CAS INDEXING IS AVAILABLE FOR THIS PATENT.
AN 1999:70581 USPATFULL
TI Method for growth of crystal surfaces and growth of heteroepitaxial single crystal films thereon
IN Powell, J. Anthony, North Olmsted, OH, United States
Larkin, David J., Valley City, OH, United States
Neudeck, Philip G., Olmsted Falls, OH, United States
Matus, Lawrence G., Amherst, OH, United States
PA The United States of America as represented by the Administrator of National Aeronautics and Space Administration, Washington, DC, United

States (U.S. government)
PI US 5915194 19990622
AI US 1997-887804 19970703 (8)
DT Utility
FS Granted
EXNAM Primary Examiner: Bowers, Charles; Assistant Examiner: Christianson, Keith
LREP Stone, Kent N.
CLMN Number of Claims: 24
ECL Exemplary Claim: 1
DRWN 11 Drawing Figure(s); 8 Drawing Page(s)
LN.CNT 1032
CAS INDEXING IS AVAILABLE FOR THIS PATENT.

L16 ANSWER 33 OF 36 USPAT2 on STN
AB LEDs employing a III-Nitride light emitting active region deposited on a base layer above a substrate show improved optical properties with the base layer grown on an intentionally misaligned substrate with a thickness greater than 3.5 .mu.m. Improved brightness, improved quantum efficiency, and a reduction in the current at which maximum quantum efficiency occurs are among the improved optical properties resulting from use of a misaligned substrate and a thick base layer. Illustrative examples are given of misalignment **angles** in the range from 0.05.**degree**. to 0.50.degree., and base layers in the range from 6.5 to 9.5 .mu.m although larger values of both misalignment angle and base layer thickness can be used. In some cases, the use of thicker base layers provides sufficient structural support to allow the substrate to be removed from the device entirely.

CAS INDEXING IS AVAILABLE FOR THIS PATENT.
AN 2002:226513 USPAT2
TI Increasing the brightness of III-nitride light emitting devices
IN Khare, Reena, Sunnyvale, CA, United States
Goetz, Werner K., Palo Alto, CA, United States
Camras, Michael D., Sunnyvale, CA, United States
PA Lumileds Lighting, U.S., LLC, San Jose, CA, United States (U.S. corporation)
PI US 6576932 B2 20030610
AI US 2001-797770 20010301 (9)
DT Utility
FS GRANTED
EXNAM Primary Examiner: Flynn, Nathan J.; Assistant Examiner: Forde , Remmon R.
LREP Patent Law Group LLP, Leiterman, Rachel V.
CLMN Number of Claims: 33
ECL Exemplary Claim: 1
DRWN 10 Drawing Figure(s); 9 Drawing Page(s)
LN.CNT 591
CAS INDEXING IS AVAILABLE FOR THIS PATENT.

L16 ANSWER 34 OF 36 USPAT2 on STN
AB A **nitride semiconductor** light emitting device includes a worked substrate including grooves and lands formed on a main surface of a **nitride semiconductor** substrate, a **nitride semiconductor** underlayer covering the grooves and the lands of the worked substrate and a **nitride semiconductor** multilayer emission structure including an emission layer including a quantum well layer or both a quantum well layer and a barrier layer in contact with the quantum well layer between an n-type layer and a p-type layer over the **nitride semiconductor** underlayer, while the width of the grooves is within the range of 11 to 30 .mu.m and the width of the lands is within the range of 1 to 20 .mu.m.

CAS INDEXING IS AVAILABLE FOR THIS PATENT.
AN 2002:111119 USPAT2
TI **Nitride semiconductor** light emitting device and apparatus including the same
IN Tsuda, Yuhzoh, Nara, JAPAN
Yuasa, Takayuki, Nara, JAPAN
Ito, Shigetoshi, Nara, JAPAN
Taneya, Mototaka, Nara, JAPAN
PA Sharp Kabushiki Kaisha, Osaka, JAPAN (non-U.S. corporation)
PI US 6452216 B2 20020917
AI US 2001-952845 20010911 (9)
PRAI JP 2000-344847 20001113
DT Utility
FS GRANTED
EXNAM Primary Examiner: Chaudhuri, Olik; Assistant Examiner: Veserman, William C
LREP Morrison & Foerster LLP
CLMN Number of Claims: 11
ECL Exemplary Claim: 1
DRWN 17 Drawing Figure(s); 10 Drawing Page(s)
LN.CNT 1163
CAS INDEXING IS AVAILABLE FOR THIS PATENT.

L16 ANSWER 35 OF 36 USPAT2 on STN
AB A **nitride semiconductor** laser device having a low threshold current and low noise is provided. The laser device includes n-type and p-type layers made of **nitride semiconductor** and formed on a substrate, and a light emitting layer between the n-type and p-type layers. The light emitting layer is formed of a well layer or a combination of well and barrier layers. At least the well layer is made of **nitride semiconductor** containing element X, N and Ga, wherein element is at least one selected from the group consisting of As, P and Sb. The atomic fraction of element X is smaller than that of N. A maximum width through which current is injected into the light emitting layer via the p-type layer is from 1.0 .mu.m to 4.0 .mu.m.

CAS INDEXING IS AVAILABLE FOR THIS PATENT.
AN 2002:105416 USPAT2
TI **Nitride semiconductor** laser device and optical device using the same
IN Tsuda, Yuhzoh, Tenri, JAPAN
Ito, Shigetoshi, Ikoma, JAPAN
Okumura, Toshiyuki, Tenri, JAPAN
PA Sharp Kabushiki Kaisha, Osaka, JAPAN (non-U.S. corporation)
PI US 6614824 B2 20030902
AI US 2001-950576 20010913 (9)
PRAI JP 2000-279207 20000914
DT Utility
FS GRANTED
EXNAM Primary Examiner: Ip, Paul; Assistant Examiner: Nguyen, Dung T.
LREP Birch, Stewart, Kolasch & Birch, LLP
CLMN Number of Claims: 12
ECL Exemplary Claim: 1
DRWN 14 Drawing Figure(s); 12 Drawing Page(s)
LN.CNT 1329
CAS INDEXING IS AVAILABLE FOR THIS PATENT.

L16 ANSWER 36 OF 36 USPAT2 on STN
AB An object of the present invention is to improve, in a group III **nitride semiconductor** device, the productivity, heat radiation characteristic and performance in the element high speed

operation; upon a sapphire substrate in which an A plane (an (11-20) plane) is set to be the basal plane, an epitaxial growth layer of a group III **nitride semiconductor** is formed and, thereon, a gate electrode 16, a source electrode 15 and a drain electrode 17 are formed; these electrodes are disposed in such a way that a direction along which they are laid makes an **angle** within 20.**degree**. with respect to a C axis of sapphire.

CAS INDEXING IS AVAILABLE FOR THIS PATENT.
AN 2002:90623 USPAT2
TI Semiconductor device having drain and gate electrodes formed to lie along few degrees of direction in relation to the substrate
IN Ohno, Yasuo, Tokyo, JAPAN
Hayama, Nobuyuki, Tokyo, JAPAN
Kasahara, Kensuke, Tokyo, JAPAN
Nakayama, Tatsuo, Tokyo, JAPAN
Miyamoto, Hironobu, Tokyo, JAPAN
Takahashi, Yuji, Tokyo, JAPAN
Ando, Yuji, Tokyo, JAPAN
Matsunaga, Kohji, Tokyo, JAPAN
Kuzuhara, Masaaki, Tokyo, JAPAN
PA NEC Corporation, Tokyo, JAPAN (non-U.S. corporation)
PI US 6441391 B2 20020827
AI US 2001-940374 20010829 (9)
PRAI JP 2000-265783 20000901
DT Utility
FS GRANTED
EXNAM Primary Examiner: Abraham, Fetsum
LREP Sughrue Mion, PLLC
CLMN Number of Claims: 3
ECL Exemplary Claim: 1
DRWN 10 Drawing Figure(s); 5 Drawing Page(s)
LN.CNT 644
CAS INDEXING IS AVAILABLE FOR THIS PATENT.

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(FILE 'HOME' ENTERED AT 08:04:46 ON 09 OCT 2003)

FILE 'HCAPLUS, INSPEC, JAPIO, USPATFULL, USPAT2' ENTERED AT 08:05:28 ON 09 OCT 2003

L1 45019 S (GAN OR GALLIUM(W)NITRIDE)
L2 34184 S (NITRIDE)(8A)(SEMICONDUCTOR)
L3 13549 S (NITRIDE(8A)CRYSTAL#)
L4 157711 S (HEXAGONAL)
L5 31516 S (CUT?)(8A)(SUBSTRATE#)
L6 39202 S (CUT? OR GRIND?)(10A)(SUBSTRATE#)
L7 357810 S (DEGREE(6A)ANGLE#)
L8 249845 S (FRONT?(8A)SURFACE#)
L9 256555 S (BACK?(8A)SURFACE#)
L10 109633 S (SCRATCH?)
L11 1370267 S (ELECTRODE#)
L12 23476 S (SUBSTRATE#)(8A)(SAPPHIRE)
L13 46 S L2 AND L3 AND L4 AND L5
L14 66 S L2 AND L3 AND L4 AND L6
L15 26 S L13 AND L7
L16 36 S L7 AND L14

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